Quartus II Software

Quick Start Guide

For the Quartus® II Software
Version 2.2

This ***Quick Start Guide*** will show you how to set up a Quartus II project, enter timing requirements, and compile the design into an Altera® device.

The Quartus II version 2.2 software introduces a new user interface based on user feedback, extensive usability testing, and the popular MAX+PLUS® II interface–designed to provide a more intuitive and user-friendly experience. In addition, the File, Project, and Processing menus have all been reorganized and restructured.

ALTERA®

Three-Step Design Compilation in the Quartus II Software

Step 1: Run the New Project Wizard (File Menu)

a. Specify project directory, name, and top-level entity.

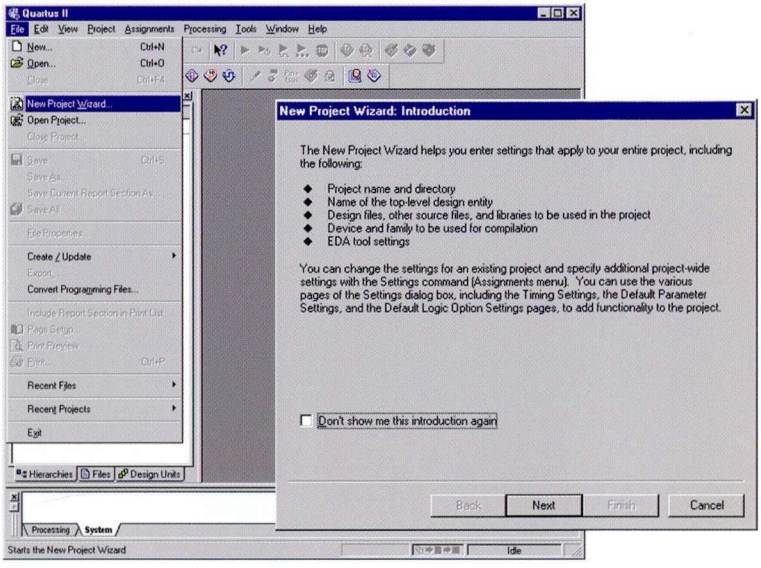
b. Specify project design files.

c. Specify other EDA tools to be used for this project.

d. Specify Altera device family for the design.

e. Specify device (or specify device information for automatic device selection).

f. Review project settings.



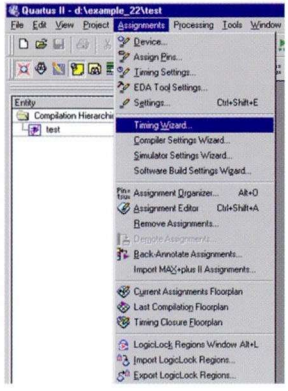
Step 2: Run the Timing Wizard (Assignments Menu)

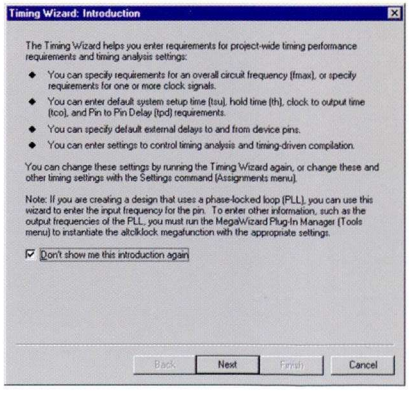
a. Specify requirements for overall circuit frequency (f_{MAX}), or specify requirements for one or more clock signals.

b. Enter project-wide system setup time (t_{SU}), hold time (t_H), clock-to-output time (t_{CO}), and pin-to-pin time (t_{PD}) requirements.

c. Specify default external delays to and from device pins.

d. Enter settings to control timing analysis and timing-driven compilation.

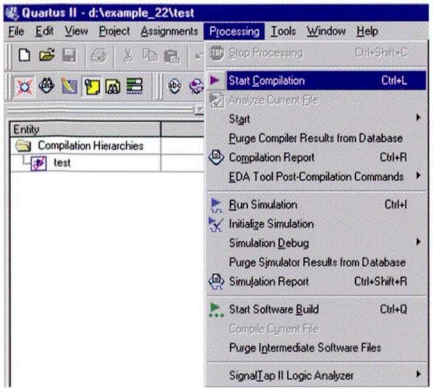


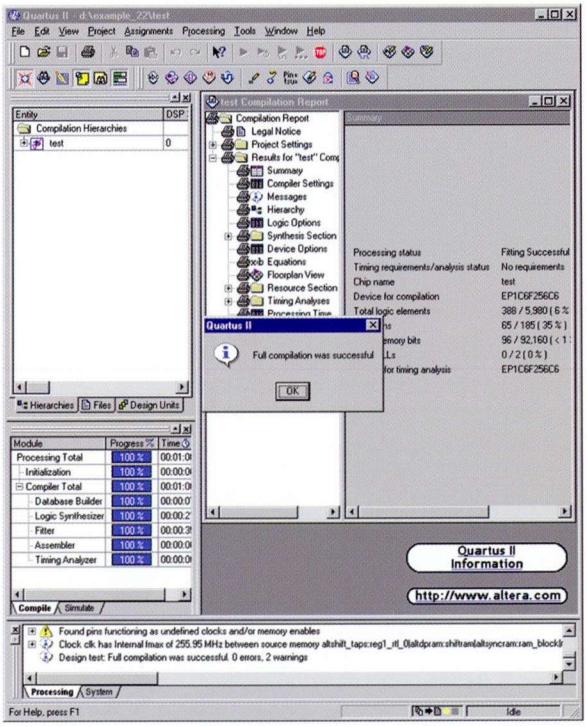


The Quartus II version 2.2 Assignments menu organizes all settings and assignments commands for the project. Choose **Settings** (Assignments menu) to view a tree-type display with access to all Quartus II settings options.

Choose **Import MAX+plus II Assignments** (Assignments Menu) to facilitate migrating a design from the MAX+PLUS® II software to the Quartus II software.

Step 3: Compile the Design (Processing Menu)





When compilation is complete, refer to the Compilation Report window to view information on compiler settings, resource usage, and compilation equations. Timing analysis is also performed during compilation on the current design, and the Compilation Report window includes timing information.

For More Information

Altera Technical Literature:
www.altera.com/literature/lit-index.html

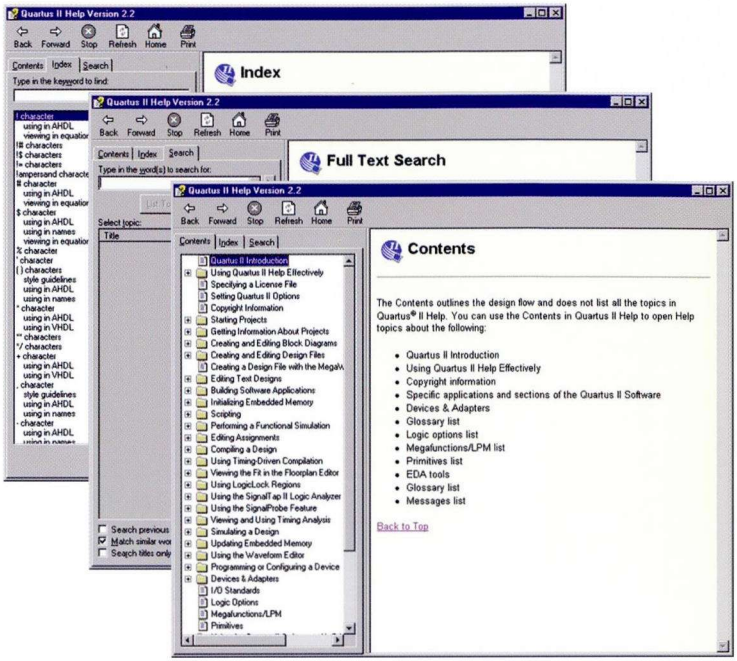
Technical Support:
www.altera.com/mysupport

Details on the Quartus II Design Flow:
www.altera.com/products/software/pld/design/qts-design_flow.html

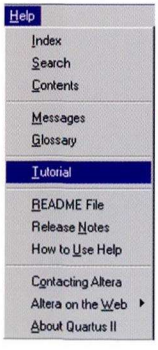
Get Quartus II Help & Information

Refer to the Quartus II Help

- Press F1 from a highlighted menu command or active dialog box for context-sensitive help
- Choose **Index** (Help menu) to view the index
- Choose **Search** (Help menu) to perform a search
- Choose **Contents** (Help menu) to view the contents



Take the Quartus II Tutorial (Help Menu)



Basic Tutorial Modules	
Module	**Description**
Design Entry	Teaches you how to create a top-level Block Design File (**.bdf**) with the Block Editor. You also create several lower-level Verilog HDL Design Files (**.v**) using the Text Editor and the **MegaWizard® Plug-In Manager**.
Compilation	Teaches you how to compile a design using Compiler settings to control compilation processing. You also learn how to view the floorplan that shows how the Compiler placed logic in the device and how to make resource and logic option assignments.
Timing Analysis	Teaches you how to analyze the timing performance of logic in a design, including how to specify timing requirements and how to perform multiclock timing analysis.
Simulation	Teaches you how to create a Vector Waveform File (**.vwf**) that contains input vectors for timing simulation and how to create Simulator settings that control simulation processing. You also learn how to perform a timing simulation.
Programming	Teaches you how to use the Quartus II Programmer to configure an Altera device.

Advanced Tutorial Modules	
Module	**Description**
Excalibur	Teaches you how to create and instantiate an ARM-based Excalibur embedded processor megafunction in a design. You also learn how to perform a functional simulation in the Quartus II software and how to build software code to run on the Excalibur embedded processor core.
LogicLock	Teaches you how to optimize a specific logic block and how to preserve the optimized constraints with the LogicLock feature of the Quartus II software. You also learn how to import the optimized block into the top-level design.
Stratix	Teaches you how to use some of the unique features of the Stratix device family, including TriMatrix memory, High-speed LVDS, and DSP blocks. You also learn how the Compiler implements the design in a Stratix device by examining the compiled design.

Use the Printing Options icon in the tutorial windows to print out any module of the on-line tutorial.